Broad-Band GaAs FET Amplifier Design Using Negative-Image Device Models

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Abstract—**A new technique is presented for determining equivalent source and load device models applicable to GaAs FET or other devices for which measured data is available. The new technique provides a more accurate starting point for matching network synthesis, better prediction of achievable circuit performance, and does not require the unilateral device assumption. Simple computer optimization and elements with negative reactance slope parameters are utilized. A description of the method and examples of its application to GaAs FET amplifier design are presented.**

I. Introduction

ADVANCES in the performance of microwave devices and the ever increasing demands on system requirements have progressed to the point where designers must be able to obtain near-optimum performance from active devices, and certainly must be able to accurately predict the maximum obtainable circuit performance for practical matching networks. Computer optimization has proven to be of enormous benefit since several "known to be practical" matching networks may be optimized in the hope of finding one for which fabrication requirements are reasonable and acceptable performance is obtained. A desirable refinement of the usual optimization technique is to use an equivalent source and load model for the device, and from network synthesis define the matching network and a starting set of element values. The overall structure is then optimized. Such procedures require no *a priori* knowledge of the matching network.

Techniques necessary to synthesize distributed matching networks in a variety of forms are readily available, as are techniques used to determine gain-bandwidth limitations for a given device model. The term "device model" is actually a misnomer when used with multiport matching network synthesis since no attempt is made to completely model a particular device. Instead, an equivalent complex impedance is determined for each port of the device such that any network designed to match into the complex load can also be connected to the appropriate device port with similar results. This artifice enables the gain-bandwidth limitations to be determined for various orders of matching networks, which immediately defines the number of sections, ripple, and minimum insertion loss which must be accepted. The complex load also determines the termination resistance at one end of the synthesized network as well as the value and type of the first element, since this portion of the network is actually the complex load.

Present procedures used to generate the device models are not accurate and/or complete enough to always permit adequate matching networks to be designed. Most existing modeling techniques assume a unilateral device and derive the equivalent model from S_{11} and S_{22}, or if noise figure is an important factor, an equivalent circuit which tracks the optimum noise impedance may be substituted for the input portion of the model. The unilateral assumption is certainly not reasonable at higher microwave frequencies, and at lower frequencies a match to S_{11} and S_{22} can very well lead to the design of an oscillator rather than the intended amplifier. Another disadvantage of existing techniques, even when some refinement is made to account for the bilateral case, is that reactive gain slope compensation is usually required, and although not difficult to synthesize, the load and source impedances which result cannot be predetermined. An appropriate selective mismatch can frequently be used to decrease VSWR, stabilize the circuit, provide a lower noise figure, or produce higher output power.

A technique using "negative-image" equivalent circuits and simple computer optimization has been developed for deriving equivalent source and load models for GaAs FET's and other devices. This technique allows device models to be derived from measured bilateral S parameters, as well as from noise and power data. The optimization error function can be weighted in the usual manner to produce the most desirable compromise between VSWR, gain, noise figure, output power, and stability. Gain-bandwidth limitation of the models can easily be included in the error function, and restrictions imposed on the resulting models to ensure that the order of the required synthesized matching network will be practical.

II. Device Modeling

The concept of negative-image equivalent source and load networks is developed in the following paragraphs. If one were *given* source and load models of a device,

Manuscript received April 24, 1979; revised June 18, 1979.

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0018-9480/79/0900-0784$00.75 ©1979 IEEE

"hypothetical" networks which would exactly match the given models at all frequencies could be generated as the topological image of the models with all model element values replaced by corresponding negative values. That such "negative-image" networks provide the desired match is easily shown in the S plane using the $ABCD$ transmission matrix, where S is either the complex frequency variable $\sigma + j\omega$ for lumped element networks, or Richards' variable $\Sigma + j\tan\beta l$ for distributed elements. Given a two-port network, form the negative image by turning the network end-for-end and replacing all elements by their negative equivalent. The cascade of the network with its negative image, the result is the identity matrix, which indicates perfect transmission, independent of frequency. Since matrix multiplication is associative, the two matrices which correspond to the positive element for the device model and the adjacent negative element of the matching network can be multiplied together to form the identity matrix, then eliminated, which again results in two adjacent positive and negative elements which can be eliminated, with as many repetitions as required.

In practice, the source and load device models are not usually known but are rather "to be determined." The desired models can be obtained from the measured device parameters using the inverse of the above procedure. Moreover, the models can easily be constrained to reflect desired overall performance characteristics such as minimum noise figure. First, a "likely" structure and trial element values for the hypothetical source and load negative-image matching networks are deduced from Immittance Plane plots of the measured device data. Next, the hypothetical networks are combined with the device (characterized by measured data), as shown in Fig. 1.

Desired performance constraints are now applied to the port characteristics of the combined structure via a computer optimization routine in which the variables are the element values of the hypothetical networks. The output of the preceding step is a pair of optimized hypothetical networks which, in combination with the actual device, produce the overall specified gain, noise figure, and/or other port constraints. Finally, the negative image looking to the left at plane 1 is the device source model under the imposed constraints. Likewise, the negative image looking to the right at plane 2 is the device load model under the imposed constraints. These models are very accurate and contain no *a priori* limitations such as the unilateral device assumption.

The optimization required in the modeling process proceeds very rapidly since the number of variables is typically small. The computer program must be able to handle negative element values. Gain-bandwidth limitation [1], [2] or minimum insertion loss and ripple can be computed for each iteration of the models, and used as a portion of the error function to ensure that the desired performance will be met with realizable synthesized networks based on the optimized models. The required matching networks

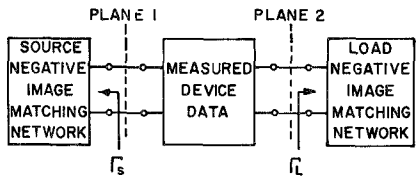

Fig. 1. Network characterization using negative-image matching networks.

are thus synthesized with the derived highly accurate source and load device models as terminations.

III. Amplifier Design

The design of a 2.0–4.0-GHz amplifier will be used to illustrate the details of this design technique. The design goals will be a 10-dB gain with less than a 2.5-dB noise figure across the band. The Hewlett-Packard HFET-1101 will be used since detailed data for both noise figure and S parameters are available. Fig. 2 shows the gain, noise figure, and stability contours mapped on the source plane. These contours indicate that there will be a problem achieving a 10-dB gain and a 2.5-dB noise figure at the low end of the band assuming a good output match; however, the gain on the source plane can be increased, which will cause the constant gain contour to fall inside the 2.5-dB noise figure circle. If this approach is taken, mismatch circles must be constructed on the output plane to compensate for the increase in low-end gain. The type of model network can be determined directly from the source and load mappings since these represent the impedance that must be presented to the device, or the impedance seen looking into the negative-image networks. In the case of the input, a positive series reactance is required which decreases with frequency. A series-connected open stub with a negative characteristic impedance in series with a resistor will meet this requirement.

An approximate value for the stub can be determined by assuming a characteristic impedance and calculating the electrical length at some frequency. The initial values selected for the source negative-image network are 30 Ω in series with an open stub, with characteristic impedance of -50 Ω and electrical length of 40 degrees at 4.0 GHz. The output model is determined in the same manner using either mismatch contours, or $S_{22}'^{*}$. Since the 10-dB gain contours were used to define the input model, the output must be matched, or the output network should present $S_{22}'^{*}$ to the device. The negative-image output model is a parallel combination of 125 Ω and an open stub of -50 Ω and 32 electrical degrees at 4.0 GHz. A schematic representation of the computer model to be optimized is given in Fig. 3.

The input and output negative-image network values are now optimized for the desired performance specification using a computer-aided design program. The resulting optimized source and load device models are shown as

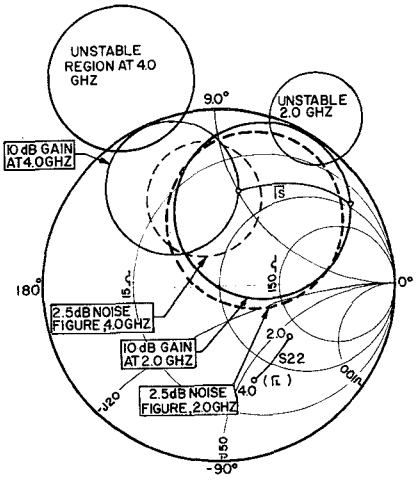

Fig. 2. HFET-1101 source plane.

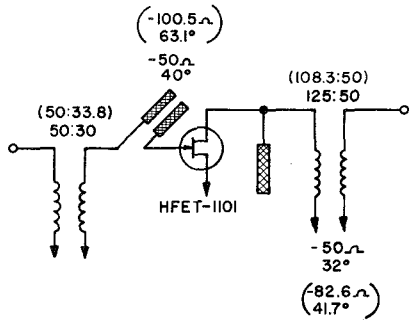

Fig. 3. Negative-image computer model.

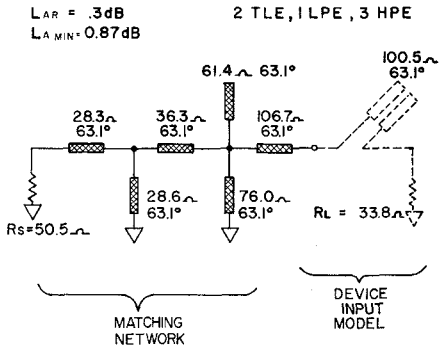

Fig. 4. Synthesized input matching network. Network topology is realizable in microstrip. Element values are realizable. Network provides ground return for the FET gate.

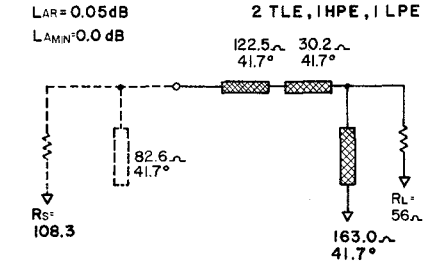

Fig. 5. Synthesized output matching network. Network topology is realizable in microstrip. Two element values are not realizable; however, since this network had a high gain-bandwidth product, constrained optimization should produce realizable values. This topology provides a convenient means of drain bias via a bypass capacitor for the single shorted stub.

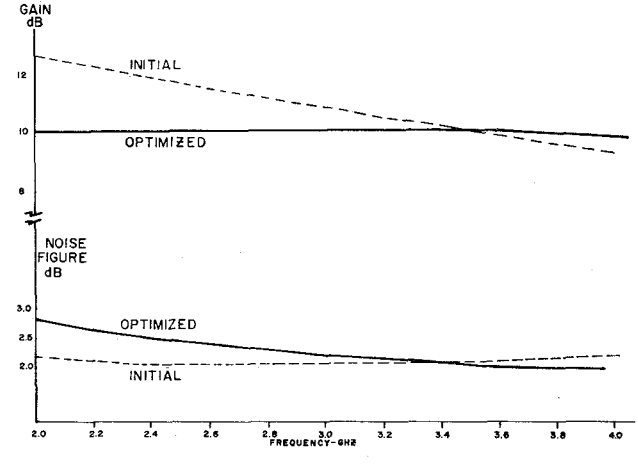

Fig. 6. Initial and optimized circuit response using negative-image matching networks.

"dotted" lines in Figs. 4 and 5, respectively. The overall optimized performance based on the ideal negative-image networks is 10 ± 0.15 dB and a maximum noise figure of 2.8 dB at the low end of the band, as shown in Fig. 6. Overall response based on nonoptimized image networks is shown for comparison. The gain-bandwidth limitation on the input network is far greater than that of the output; therefore, the input matching network will be synthesized and then optimized while the output remains in the image model form. This approach increases the optimization speed since fewer variables are required.

Several distributed synthesis procedures are useful for the matching network design. Levy's technique [3] for impedance transforming filters and the work of Mokari-Bolhasson and Ku [4] have been incorporated in a minicomputer-based synthesis program. The technique of [4] has been modified to allow for the synthesis of generalized structures with specified commensurate line length. Several networks can easily be investigated for physical realizability and the desired termination impedance. In some cases, partial element extraction can also be used to adjust the termination impedance.

Based on the optimized input model, an input matching network with two transmission-line elements, one low-pass element, and three high-pass elements was synthesized for 0.3-dB Chebyshev ripple and 0.87-dB minimum insertion loss. Partial element extraction was used to adjust the termination impedance to 50.5 Ω and a nonminimum transmission-line element was extracted to allow easier physical realization. Many other networks may be synthesized to match this source device model. The network shown as "solid" lines in Fig. 4 is quite satisfactory since the element values are realizable and the structure has a shorted stub which can be used to ground the FET gate.

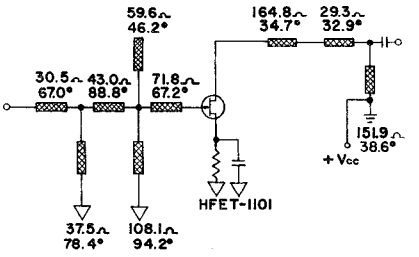

Fig. 7. Final amplifier.

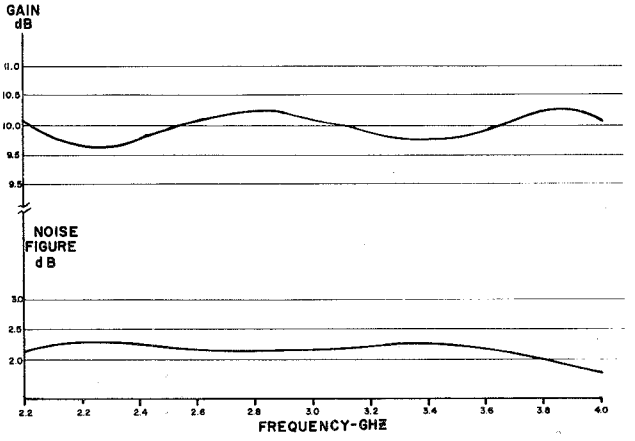

Fig. 8. Gain and noise figure performance of final amplifier.

Optimization of the distributed structure provides improved performance over the synthesized network since an additional degree of freedom is added when the line length is allowed to vary. The results from the optimization of the input matching network and output negative-image model meet all the performance specifications, the gain is exactly 10.0 dB and the maximum noise figure is 2.4 dB at 2.0 GHz. The output model resulting from this process is shown in Fig. 5 along with the synthesized matching network. This network has 0.05-dB Chebyshev ripple and zero minimum insertion loss with a termination impedance of 56 Ω. The final optimized amplifier circuit is shown in Fig. 7.

The performance which is obtained from this design is a 10.0 ± 0.3-dB gain with a noise figure of less than 2.3 dB across the 2.0–4.0-GHz band, as shown in Fig. 8. The next step should be to constrain the impedance values to realizable levels and again optimize using a constrained search. This will not effect the performance to any significant degree since the element values which may be difficult to realize are in the output network which has a high gain-bandwidth product. The final step involves modeling all parasitics and losses which can be identified, and perform one last optimization on only those variables which do not effect the parasitic values.

IV. 7–18-GHz Measured/Computed Results

A 7–18-GHz GaAs FET amplifier based on the 0.5-μ NEC device has been designed using negative-image device modeling. Fig. 9 illustrates the high degree of correlation between the measured amplifier performance and the computer predicted response. Nominal gain is 5 dB. Noise figure is less than 7 dB over the 7–18-GHz band. Even outside the band of interest, measured response closely follows calculated values. A photograph of the final unit (0.9 in × 2.25 in × 0.7 in) is shown in Fig. 10.

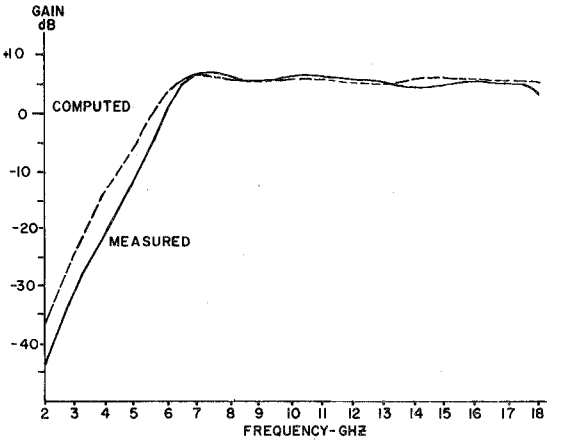

Fig. 9. Computed versus measured response for a 7.0–18-GHz amplifier designed using the negative-image technique.

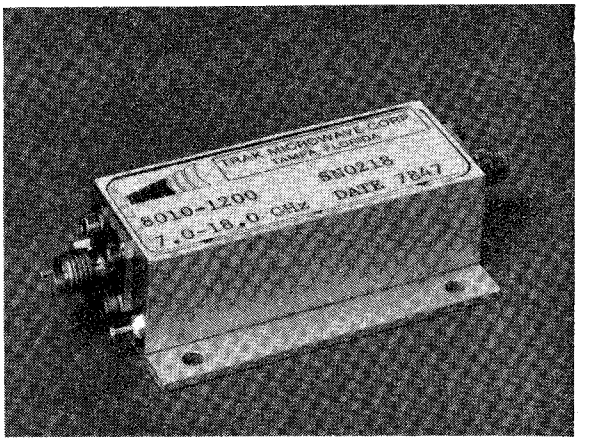

Fig. 10. The final 7.0–18.0-GHz amplifier.

V. Conclusion

A technique for deriving highly accurate source and load device models from measured device data has been described. The technique which is based on "negative-image" networks does not require a unilateral device assumption and constraints representing a compromise of several device characteristics can easily be imposed. The negative image modeling technique has proven to be an excellent design tool for broad-band GaAs FET amplifiers.

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Optimization of Interdigital Capacitors

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***Abstract*—The variation of Q and capacitance slope for series- and shunt-connected interdigital capacitors is shown. A theory suitable for interactive design of capacitors is given.**

I. Introduction

THE use of interdigital capacitors on microstrip has become common place over the past few years [1], but little work has been published on the performance of the capacitors at X–J-band frequencies. Three factors must be considered when designing an interdigital capacitor, namely: capacitance slope, Q, and parasitics. This paper describes the effect of the interdigital capacitor layout on the first two factors.

II. Theory

Alley [2] has shown how a two-port matrix may be derived and used to represent a shunt-connected capacitor. This is the case where one side of the capacitor is grounded. Here the more general case of a series-connected capacitor, where both sides are used, is considered. In this case a four-port matrix is used to represent the capacitor and to determine the effect of changes in the capacitor shape.

Consider a pair of fingers of an interdigital capacitor (Fig. 1). Then a two-port admittance matrix $[Y_f]$ can represent the finger ports [3]. The elements of $[Y_f]$ are given by

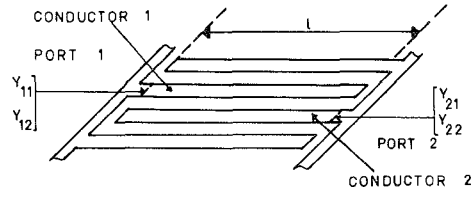

Fig. 1. Central form of an interdigital capacitor.

where Zo_o and Zo_e are the odd- and even-mode impedances; γ_o and γ_e are the odd- and even-mode propagation constants; and l is the length of overlap of the fingers.

The impedances Zo_o and Zo_e were calculated using the computer program given by Smith [4] to compute the odd- and even-mode capacitances of the lines. Smith considers the case of a triplet of lines and obtains one pair of odd- and even-mode capacitances for the center line, and another pair for the outer lines. The values for the center lines were used to evaluate (1) and (2).

The loss components α_e, α_o for the propagation constants γ_o, γ_e were calculated using the formulas given by Schneider [5], but no allowance was made for surface roughness [6]. The formulas of Schneider assume a single-mode TEM transmission line. In order to use these formulas, it was assumed the coupled line loss components could be represented by two TEM-mode transmission lines of characteristic impedance Zo_o and Zo_e. A similar method was used by Horton [7] who shows the odd-mode component loss to be predominant. The result of these approximations is that the Q will take an optimistic value but show the correct variation for changes in shape of the interdigital capacitor.

$$y_{11}=y_{22}=\frac{2\left[Zo_e\coth(\gamma_e l)+Zo_o\coth(\gamma_o l)\right]}{Zo_o^2+Zo_e^2+2Zo_oZo_e\left[\coth(\gamma_o l)\coth(\gamma_e l)+\operatorname{csch}(\gamma_o l)\operatorname{csch}(\gamma_e l)\right]} \tag{1}$$

$$y_{21}=y_{12}=\frac{-2\left[Zo_e\operatorname{csch}(\gamma_e l)-Zo_o\operatorname{csch}(\gamma_o l)\right]}{Zo_o^2+Zo_e^2+2Zo_oZo_e\left[\coth(\gamma_o l)\coth(\gamma_e l)+\operatorname{csch}(\gamma_o l)\operatorname{csch}(\gamma_e l)\right]} \tag{2}$$

Manuscript received October 1, 1976; revised November 11, 1978. This work was supported by Science Research Council.

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0018-9480/79/0900-0788$00.75 ©1979 IEEE